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10/764,967	01/26/2004	Dale E. Parson	5	9305

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EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/764,967	PARSON, DALE E.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/10/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-30 are in the application.

Claims 1-30 are rejected.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

A person shall be entitled to a patent unless -

(a) the invention was known or used by other's in this country or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another fled in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-5,10,23-25 rejected under 35 U.S.C. 102 (e) as being anticipated by Crawford et al (US 5918055).

As in claim 1, Crawford describes a method for resource management in a processor-based system (Fig 2: #28 token based request processor, controller), the method comprising the steps of: storing a plurality of data values in a hardware queue (Fig 2: FBQ free buffer queue; column 3 lines 57-67 digital agent 22, token-based responder push the token into the free-buffer queue; Fig 2: VRQ), each data value being associated with a corresponding one of a plurality of resources (Fig 2: #32 memory; column 3 lines 44-57 describes the corresponding packet information being placed in memory #32), wherein presence of a given one of the data values in the hardware queue indicates availability of its corresponding resource to a requesting object; and utilizing the given data value from the hardware queue to access the corresponding resource (column 3 lines 30-44, token-based controller has priority knowledge of the available and identify of buffer resource; if a token is available in the free buffer queue, that means there is a digital resource available to accept the packet).

As in claim 2, Crawford describes the step of reading the given data value from the hardware queue (column 3 lines 30-44).

As in claim 3, Crawford describes wherein the step of reading at least partially allocates the given resource by removing the given data value from the plurality of data values in the hardware queue, thereby providing access to the corresponding resource by the requesting object of a plurality of objects in the processor-based system and preventing access to the corresponding resource for other objects in the processor-based system (Crawford's column 4 lines 11-50).

As in claim 4, the claim recites in conjunction with the step of reading, the step of the hardware queue removing the given data value from the plurality of data values. Crawford describes removes a token value from the tokens in the free buffer queue, column 3 lines 35-44.

As in claim 5, the claim recites the step of writing the given data value to the hardware queue. Crawford describes writing a token value into the free buffer queue, column 3 lines 60-68.

As in claim 10, the claim recites wherein the step of utilizing further comprises the step of mapping the given data value to its corresponding resource (Crawford's column 5 lines 20-68).

As in claim 23, the claim recites wherein the one or more processors are adapted to read the given data value from the at least one hardware queue during a read operation, wherein the hardware queue is adapted, in conjunction with the read operation, to remove the given data value from the plurality of data values, thereby providing access to the corresponding resource by the requesting object of a plurality of objects and preventing access to the corresponding resource for other objects. The claim rejected based on the same rationale as in the rejection of claim 4.

As in claim 24, the claim recites wherein the one or more processors are adapted to write the given data value to the at least one hardware queue during a read operation, wherein the at least one hardware queue is adapted, in conjunction with the write operation, to add the given data value to the plurality of data values, thereby providing access to the corresponding resource by providing access to the given data value. The claim rejected based on the same rationale as in the rejection of claim 3.

As in claim 25, the claim recites wherein the one or more processors are further adapted, in conjunction with utilizing the given data value, to map the given data value to its corresponding resource. The claim rejected based on the same rationale as in the rejection of claim 10.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-9,11-12,16-22,26-30 rejected under 35 U.S.C. 103(a) as being unpatentable over Crawford et al (US 5918055).

As in claims 6-7, the claim recites wherein the step of writing at least partially recovers the corresponding resource by adding the given data value to the plurality of data values in the hardware queue, thereby providing access to the given data value and its corresponding resource for any object of a plurality of objects in the processor-based system (claim 6); in conjunction with the step of writing, the step of the hardware queue adding the given data value to the plurality of data values (claim 7). Crawford describes the hardware adding the token into the

toke-based available queue so that it is available for other requesters (Crawford's column 3 lines 60-67; column 4 lines 12-48).

As in claim 8, wherein each of the plurality of data values comprises a bit pattern uniquely corresponding to one of the resources. Crawford's column 5 lines 22-67.

As in claim 9, the claim recites wherein: the hardware queue is accessed through a data bus (Fig 1: #20 data transmission channel); the hardware queue comprises a queue memory and read and write interfaces; the read interface reads from the queue memory and the write interface writes to the queue memory; both the read and write interfaces are coupled to the data bus (Fig 4 full duplex 3 ports switching system, column 5 lines 15-25); and the queue memory is configured to store the plurality of data values (Fig 2: FBQ,VRQ, column 3 lines 35-68).

As in claim 11, the claim recites wherein each of the plurality of data values comprises a database key that corresponds to a portion of application data, and wherein the step of mapping further comprises the step of mapping the given data value to a corresponding portion of the application data. Crawford describes of assigning token values to identify the requests for resources such as portions of data in a memory that is shared among tasks being executed in a multi-processors environment (Crawford's column 5 lines 1-10, column 6 lines 1-17). Furthermore, it has been known in the art that an application can be processed by multiple processors in a concurrently manner.

As in claim 12, the claim recites wherein each of the database keys comprises an index, the application data comprises hardware identifiers and wherein the step of mapping further comprises the step of mapping the given data value to a corresponding hardware identifier. The claim rejected based on the same rationale as in the rejection of claim 11. Crawford further

describes the assignment of identified packet to a buffer slot in memory resource using token value in the available free queue (Crawford's column 3 lines 35-40).

As in claim 16, the claim recites wherein: each of the database keys comprises an index identifying an address range of a memory; and the step of mapping further comprises the step of mapping the given data value to a given address range of the memory. (Crawford's column 3 lines 45-52).

As in claim17, the claim recites reading the hardware queue a plurality of times to retrieve a plurality of read data values from the plurality of data values; writing the plurality of read data values to a predetermined portion of a memory; and reading at least one of the read data values from the predetermined portion of the memory. The claim rejected based on the same rationale as in claim 1. Crawford further describes the token-based requests allowing asynchronous agents to process requests as soon as the buffers are available; they are lock-free communications among requests agents (Crawford's column 2 lines 10-38; column 7 lines 1-5).

As in claim 18, the claim recites the steps of: writing a plurality of written data values to a predetermined portion of a memory; reading at least one of the written data values from the predetermined portion of the memory; and writing the at least one written data value to the hardware queue to add the written data value to the plurality of data values. The claim rejected based on the same rationale as in the rejection of claim 17.

Claim 19 rejected based on the same rationale as in the rejection of claims 1 and 9.

Claims 20,26 rejected based on the same rationale as in the rejection of claims 19.

Claim 21 recites an integrated circuit comprising: at least one hardware queue connectable to one or more processors via a data bus, the at least one hardware queue configurable to store a plurality of data values; and the one or more processors adapted, for the at least one hardware queue: to store a plurality of data values in the at least one hardware queue, each data value being associated with a corresponding one of a plurality of resources, wherein presence of a given one of the data values in the at least one hardware queue indicates availability of its corresponding resource to a requesting object; and to utilize the given data value from the at least one hardware queue to access the corresponding resource. Claim 21 rejected based on the same rationale as in the rejection of claim 19. Crawford's Fig 4, Fig 1, column 4 lines 15-35 further shows a switching system including token based-processor, memory, queue, and controller.

As in claim 22, the claim recites wherein the at least one hardware queue comprises a plurality of hardware queues, each of the plurality of hardware queues being associated with a given set of resources of a plurality of sets of resources (Crawford's column 5 lines 10-22, multiple memory regions for each digital resource; column 4 lines 27-40, multiple valid request queues, multiple free buffer queues of the same or different physical interfaces).

Claim 27 rejected based on the same rationale as in the rejection of claims 3,4.

Claim 28 recites wherein the at least one processor is adapted: to store the plurality of data values in the at least one hardware queue, each data value being associated with a corresponding one of a plurality of resources, wherein presence of a given one of the data values in the at least one hardware queue indicates availability of its corresponding resource to a requesting object; and to utilize the given data value from the at least one hardware queue to

access the corresponding resource. Claim 28 rejected based on the same rationale as in the rejection of claim 27.

As in claim 29, the claim recites wherein the integrated circuit comprises the plurality of resources, the plurality of resources are external to the integrated circuit, or at least part of each resource of the plurality of resources resides on the integrated circuit. Crawford Fig 4,2 shows memory resource resides in the switch system.

As in claim 30 the claim recites an address bus; and at least one queue enable module coupled to the address bus and to the at least one hardware queue, the at least one queue enable module adapted to enable the at least one hardware queue when an address on the address bus corresponds to an address associated with the at least one hardware queue. Crawford describes the data transmitting on the data transmission channel including information such as associated buffer ID (memory address) that identifies unique buffer in the system (Crawford's column 5 lines 27-35. Crawford teaches the token-based requests can be applied to manage digital resources communicating over a system bus (Crawford's column 1 lines 25-35). Furthermore, it has been known in the art that the system bus between processors, I/O devices and main memory would have address and data buses to provide address and data to access the memory component.

Claims 13-14 rejected under 35 U.S.C. 103(a) as being unpatentable over Crawford et al (US 5918055) as applied to claim 11, and in view of Joseph et al (US 6628615).

As in claim 13, the claim recites wherein: each of the database keys comprises an integer; the application data comprises connection identifiers; and the step of mapping further comprises the step of mapping the given data value to a corresponding connection identifier. Although

Crawford describes that digital agents (a network), routers and processors forward packets in the network using the token's information to determine source and destination of the packets (Crawford's column 5 lines 23-67). Crawford does not explicitly describe the claim's aspect of a connection identifier. However, Joseph describes the method to send the packets in the networks that have channel id, node id, end point id, that are recorded in a connection state stable (Joseph's column 5 lines 24-37). It would have been obvious to one of ordinary skill in the art at the time of invention to include connection method and channel identifier data structures as suggested by Joseph in Crawford's system thereby allowing packets from different sources concurrently transmitted over a physical channel (Joseph's column 2 lines 5-14).

As in claim 14, the claim recites the step of allocating a plurality of portions of a connection status table (Joseph's column 5 lines 30-35); each of the database keys comprises an index identifying a portion of a connection status table; and the step of mapping further comprises the step of mapping the given data value to a portion of the connection status table (Joseph's column 5 lines 36-65, indexing into the address of the payload).

Claim 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Crawford et al (US 5918055) as applied to claim 11, and in view of Huang (US 2004/0201592).

As in claim 15, the claim recites wherein: each of the database keys comprises an integer corresponding to a hardware thread identification; and the step of mapping further comprises the step of mapping the given data value to a local storage memory location corresponding to the hardware thread identification. The claim rejected based on the same rationale as in the rejection of claim 12. Crawford does not describe the claim's detail of the mapping data values. However,

Huang describes a graphic system capable of processing multiple data streams concurrently, the system has a controller that selects a memory to store the primitive's information, the memory has a corresponding thread ID as an identifier to the memory (Huang's paragraph 6). It would have been obvious to one of ordinary skill in the art at the time of invention to include the mapping of thread ID as an identifier for the object occupying the corresponding memory as suggested by Huang in Crawford's system therefore allowing to process objects concurrently and still maintain the ordering as they arrived for processing, thereby improve the overall throughput and allowing efficiently use of the available memory (Huang's page 1 paragraphs 5,6; page 2 paragraph 8).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

McGee et al (US 6877077).

Wolrich et al (US 6587906).

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DD

Mano Padmanabhan 3/20/06

Supervisory Patent Examiner

TC2188

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER